



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,865	12/12/2001	Ronald A. Sartshev		2596

7590

02/26/2004

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER


PHAN, THANH S

ART UNIT	PAPER NUMBER
----------	--------------

2841

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/015,865	Applicant(s) SARTSCHEV ET AL. 	
	Examiner Thanh S Phan	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/11/02 and 4/22/03</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 4, line 4, applicant should clarify what the coincidence reflects. It appears that the claim is incomplete.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sarschev et al. [6,073,259] in view of Chu [4,164,648] and Murakami [5,872,745].

Regarding claims 1, 9-10, 12 and 18-19, Sarschev et al. disclose a time measurement circuit are use within automatic test equipment comprising a clock signal [116]; a plurality of delay elements [212(0)-212(16)] forming a delay chain having an input [figure 2a] connected to the clock wherein each of the element having a tap [DO] to select the output of each delay element.

Sarschev et al. disclose every claimed except for the use of a second plurality of delay elements each having an input and output coupled to the stop input and a coincidence circuit having a first plurality of inputs each coupled to one of the taps and a second plurality of inputs each coupled to the output of one of the second plurality of delay and an output with the output representing the coincidence between one of the taps and one of the outputs of the second plurality of delay elements.

Chu discloses the use of a vernier type control circuit for regulating a timing sequence comparing the outputs of multiple delay elements [column 6, lines 11-43].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the delay element structure of Chu for the system of Sarschev in order to sequence the chip testing operation.

Murakami discloses the use of a coincidence circuit [112] comparing the outputs of a plurality of signals obtained through different stages of delay buffers [105] for carrying out zero detection based output values.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the coincidence circuit design of Murakami with the outputs derived from measurement circuit of Sarschev et al., as modified, in order to detect defects in the automated test.

Regarding claims 2-5 and 14, Murakami discloses the coincidence circuit utilizing a plurality column circuits and logic circuits comparing the outputs connected to the taps to reflect coincidence of the inputs [column 1, line 63-column 2, line 15].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use comparison technique of Murakami in Sarschev et al., as modified, for purpose of providing indication of a defect.

Regarding claims 6-7, Murakami further discloses the use of a comparison circuit to compare the outputs of the delay element outputs [column 2, lines 16-24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use comparison technique of Murakami in Sarschev et al., as modified, for the purpose of controlling the timing sequence.

Regarding claims 8 and 15, Sarschev et al. discloses a calibration circuit [226] and storage means therefor [column 5, lines 34-48].

Regarding claims 11 and 13 Sarschev et al. discloses the use of a delay locked loop controlling the output of the delay line [column 4, line 66-column 5, line 10].

Regarding claims 16-17 and 20, Sarschev et al. disclose the measurement circuit implemented on a CMOS chip [figure 3].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ichimiya et al. [US 4402081] ; Staiger [US 5,479,415] ; Zhevnerov [US 4,104,590].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh S Phan whose telephone number is 571-272-2109. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David S Martin can be reached on 571-272-2107. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tsp

A handwritten signature in black ink, appearing to be 'D. Martin', written in a cursive style.

DAVID MARTIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800